

MULTIPLE CHIP SYSTEM INCLUDING A PLURALITY OF NON-VOLATILE SEMICONDUCTOR MEMORY DEVICES

Abstract of the Disclosure

A multiple chip memory system capable of providing state information relating to each chip embedded therein. The multiple chip memory system includes a first chip enabled by a first chip selection signal, and informing of a self state by a first ready/busy signal; and a second chip enabled by a second chip selection signal, and informing of a self state by a second ready/busy signal.